

Digital systems and design

LAB # 3



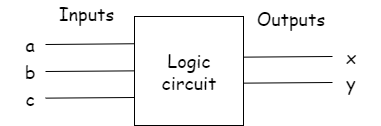
February 18, 2024

NAQI UL HASSAN

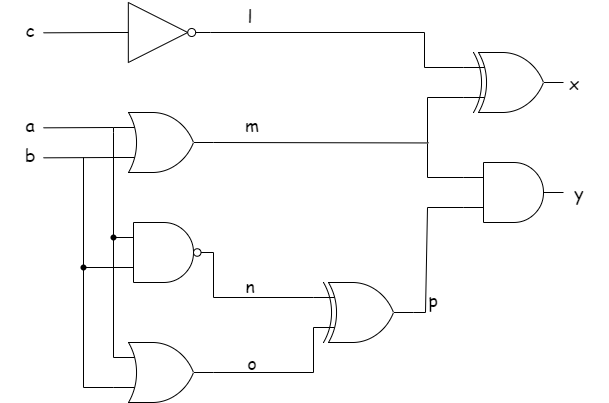
2022-EE-164

Lab Report

Inputs/Outputs:



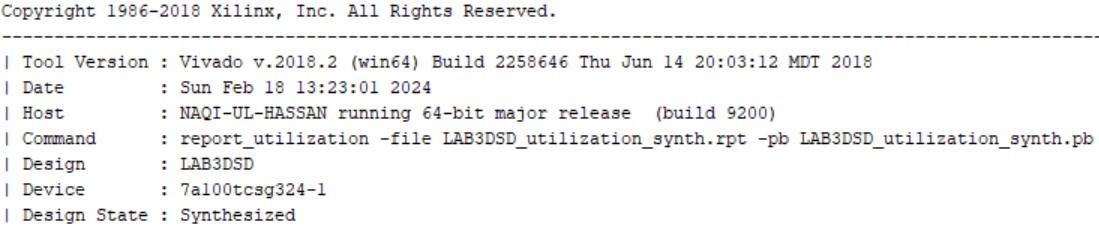
Circuit Diagram:



Task 1(a):

Truth table of the given circuit

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | |  | | | | | **Outputs** | |
| **a** | **b** | **c** | **l** | **m** | **n** | **o** | **p** | **x** | **y** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

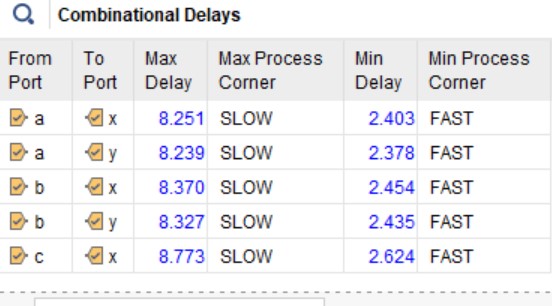


Task 1(b):

Maximum combinational delay in synthesis is from port **c** to **y** i.e. almost 8.773ns.



And following are the combinational delays:

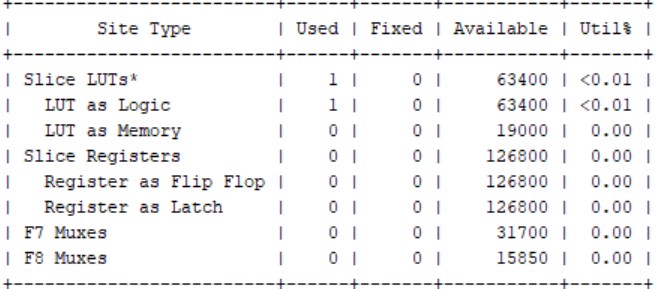


Task 1(c):

Following are the resource utilizations:

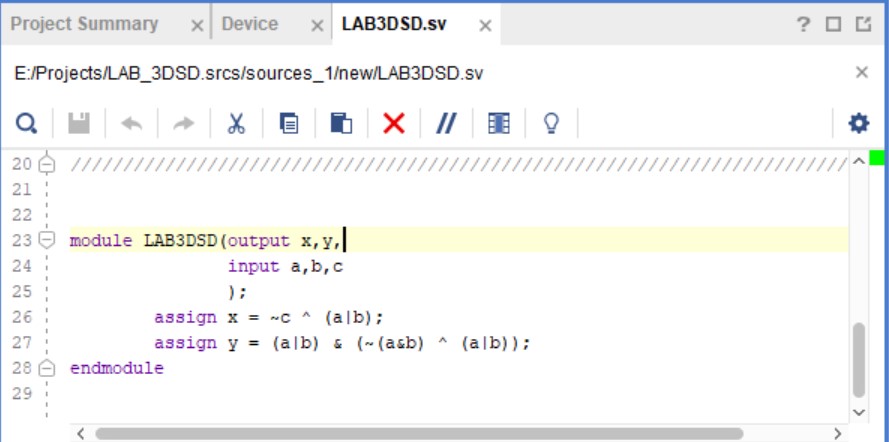
* Slice LUT’s and LUT’s logic
* I/O ports are used

For input I have used switches and for output I have used LED ports.

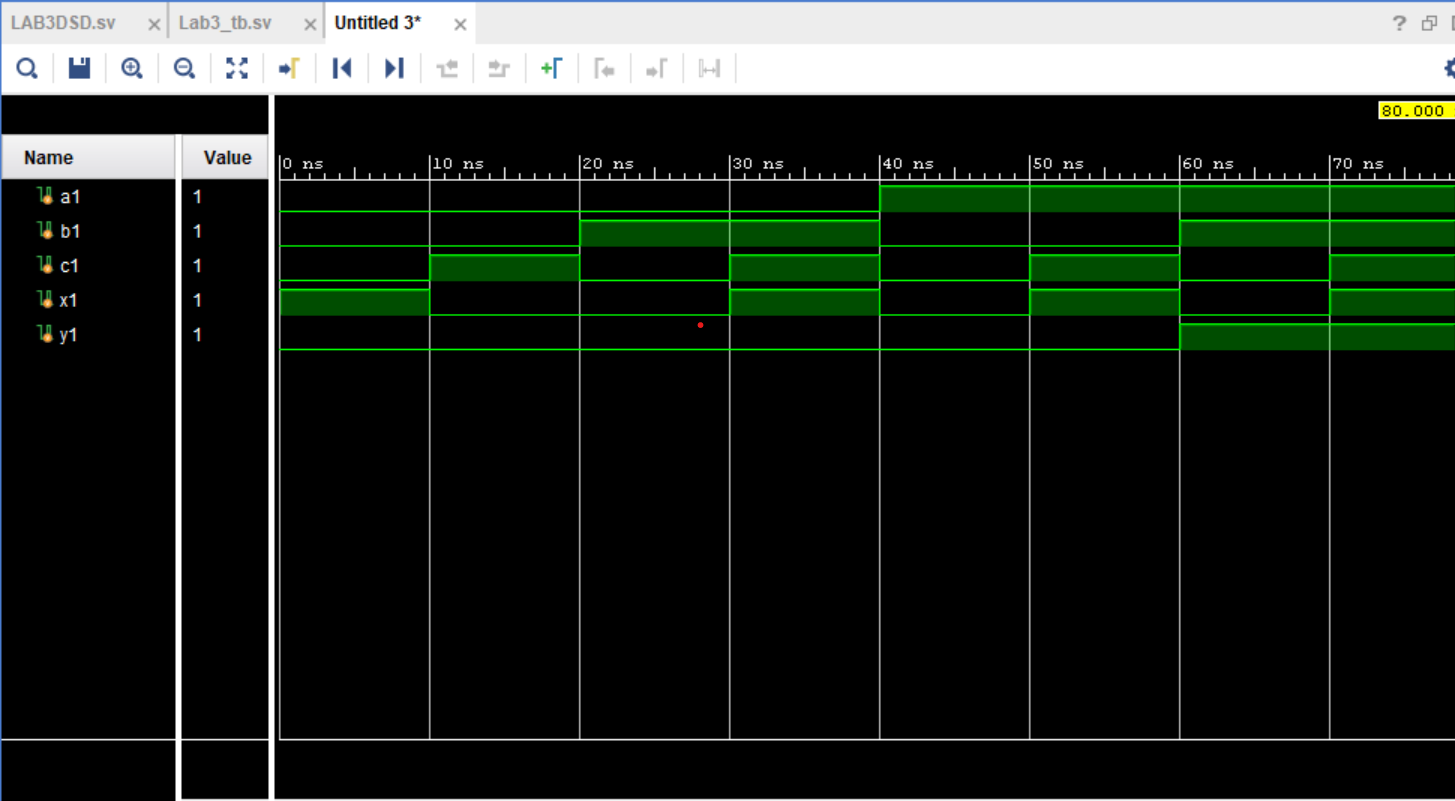


Task 2:

This is the system Verilog file:



And here is the wave form generated by it:



And its test bench code is:

